Abstract of the Disclosure

METHOD FOR INCREASING EFFICIENCY IN A MULTI-PROCESSOR SYSTEM AND MULTI-PROCESSOR SYSTEM WITH INCREASED EFFICIENCY

A multi-processor system includes a system bus communicating between processors, and a bus arbiter. Responsive to a cache line invalidation command, a processor cache conditionally casts back the cache line to a transition cache. Based on the system response to the invalidation command, the transition cache either discards the cast back or writes it to main memory. The processor also converts an exclusive read command requiring a reservation to non-exclusive if the reservation has been lost before placing the command on the system bus. Furthermore, the transition cache may shift memory coherency image state for a non-exclusive command, which is waiting for data to return, if a command involving the same real address is snooped. Responsive to a cache line request, the cache copies that cache line to the transition cache and updates cache line state. The transition cache holds the cache line pending system response.